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Harmonic Reduction in Induction Motor: Multilevel Inverter

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Abstract

The cascaded multilevel inverter (CMLI) possesses acquired significantly consideration nowadays due to their positive aspects in substantial voltage as well as excessive power with minimal harmonics purposes. The bad quality of voltage as well as current of a traditional Inverter feasted Induction machine is on account of the availability of harmonics. This is exactly overwhelmed in multilevel inverter with significant measures which may produce premium quality voltage waveforms .The multilevel inverter output possesses diminished harmonics and also greater torque. Moreover it minimizes the heat produced in the stator winding of the induction motor. A regular cascaded multilevel inverter necessitates requires n DC suppliers for 2n+1 range at the output, exactly where n is the quantity of inverter levels. Without having to use Pulse Width Modulation (PWM) strategy, the firing circuit may be executed utilizing PWM strategies tremendously cuts down the Total Harmonic Distortion (THD) and also switching deficits. Multilevel inverter utilizing Selective Harmonic Elimination (SHE) technique can be simulated along with the respective outcomes is obtainable. The FFT spectrum for the outputs is examined to analyze the lowering of harmonics. Multilevel inverter is always to synthesize a close to sinusoidal voltage from a number of stages of dc voltages. Multilevel inverter possesses convenience like minimum amount harmonic distortion. To establish the make and model of a cascaded hybrid multilevel inverter and a demonstration is performed according to MATLAB/SIMULINK software. Their integration tends to make the model as Well as evaluation of a hybrid multilevel inverter.

Keywords: *Multilevel inverter, Cascaded inverter, Digital control, Total Harmonic distortion, switching losses.*

1. Introduction

Power electronic converters, especially dc/ac PWM inverters have been extending their range of use in industry because they provide reduced energy consumption, better system efficiency, and improved quality of product, good maintenance and so on. It should be noted that lower switching frequency usually means lower switching loss and higher efficiency. Large electric drives and utility applications require advanced power electronics converter to meet the high power demands. As a result, multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations[1]. A multilevel converter not only achieves high power ratings, but also improves the performance of the whole system in terms of harmonics, d_v/d_t stresses, and stresses in the bearings of a motor. Several multilevel converter topologies have been also developed i) diode clamped, ii) flying capacitors, and iii) cascaded or H-bridge. Referring to the literature reviews, the cascaded multilevel inverter (CMI) with separated DC sources is clearly the most feasible topology for use as a power converter for medium & high power applications due to their modularization and extensibility[2]. The H-bridge inverter eliminates the excessively large number of (i) bulky transformers required by conventional multilevel inverters, (ii) clamping diodes required by multilevel diode-clamped inverters and (iii) flying capacitors required by multilevel flying-capacitor inverter. As a preliminary study the thesis examined and compared the most common multilevel topologies found in the published literature[3]. Starting from the essential requirements, the different approaches to the construction of multilevel inverter are explained and compared. In particular, aspects of total harmonic distortion (THD) and modulation which are required or desirable for multilevel converters are discussed[4]. Sine-triangle carrier modulation is identified as the most promising technique to pursue for both technical and pedagogical reasons. Since cascaded multilevel inverter is considered to be suitable for medium & high power applications, the harmonic analysis of 3-level, 5-level, & 7 level cascaded multilevel inverter induction motor drives through analysis, simulation & experiment[5]. As alternatives to effectively solve the above-mentioned problems, several circuit topologies of multilevel inverter and converter have been researched and utilized. The output voltage of the multilevel inverter has many levels synthesized from several DC voltage sources. The quality of the output voltage is improved as the number of

voltage levels increases, so the quantity of output filters can be decreased[6]. The elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform[7]. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple dc voltage sources. The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at the output however, the rated voltage of the power semiconductor switches depends only upon the rating of the dc voltage sources to which they are connected.

A multilevel converter has several advantages over a conventional two-level converter that uses high switching frequency Pulse Width Modulation (PWM).Staircase waveform quality: Multilevel converters not only can generate the output voltages with very low distortion, but also can reduce the d_v/d_t stresses; therefore electromagnetic compatibility (EMC) problems can be reduced[8].

Multilevel inverters have drawn tremendous interest in the power industry. They present a new set of feature that are well suited for use in reactive power compensation. Multilevel inverters will significantly reduce the magnitude of harmonics and increases the output voltage and power without the use of step-up transformer. A multilevel inverter consists of a series of H-bridge inverter units connected to three phase induction motor. The general function of this multilevel inverter is to synthesize a desired voltage from several DC sources. The AC terminal voltages of each bridge are connected in series[9].

2. Cascaded multilevel inverter

The cascaded H-bridges inverter consists of H-bridges in series configuration. Such technology is very attractive for application such as [6-7] motor drive systems, power distribution, power quality and power conditioning application. Each H-bridge inverter module can generate three different output voltage levels namely 0, +Vdc and -Vdc. The multilevel inverter of Fig.1 utilizes two independent DC sources and consequently will create an output phase voltage with seven levels. N is the number of independent DC sources per phase, m is the number of levels, l represents the number of switches with freewheeling diodes per phase, then the following equations are applied for CMLI : A simplified single phase topology is shown in Fig. 2.1.The output voltage will be +10V (top inverter H1) when switches T11 and T14 conducts. Similarly, 10V will be obtained when T12 and T13 conducts. The output voltage is +20V only when T21 and T24 are conducting and the output voltage is -20V only when T22 and T23 are conducting. The output voltage +30V is available when switches T11, T14 ,T21 and T24 conducts and -30V is available when switches T12,T13 T22 and T23 conducts.

3. Purpose of Harmonic Reduction

The output voltage of multilevel inverter is a symmetric stepped voltage waveform. The output voltage will have fundamental and the associated harmonics. The dc link supply for each full bridge converter is provided separately, and this is typically achieved using these harmonics produce additional heating, when the output voltage of the inverter is fed to the load. Therefore in order to reduce that, harmonic reductions is necessary.

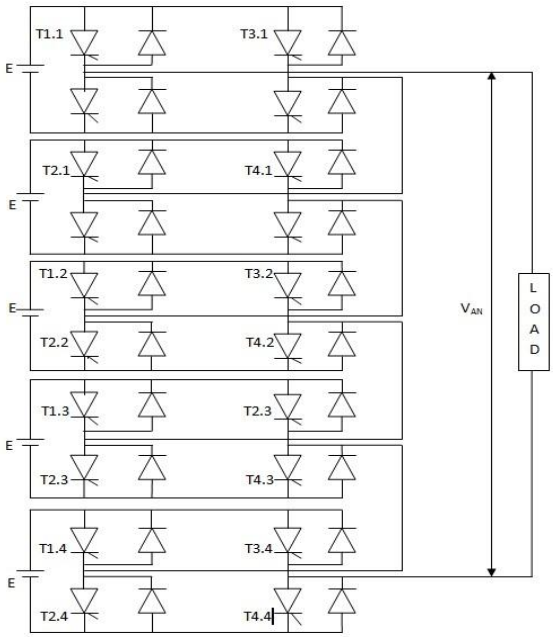

Fig. 1 Eleven Level Cascaded H-Bridge Topology

Each level can generate eleven different voltage outputs by connecting the dc sources to the ac output side by different combinations of the eleven switches. The number of output phase voltage levels m in a cascade inverter is defined by m = 2s+1, where s is the number of separate dc sources. The 11-levels of voltages are 0, V/5, 2V/5, 3V/5, and 4V/5, V, -V/5, -2V/5, -3V/5, -4V/5,-V. The output voltage of an M-level inverter is the sum of all the individual inverter outputs. Each of the H-Bridge's active devices switches only at the fundamental frequency, and each H-bridge unit generates a quasi- square waveform by phase-shifting it's positive and negative phase legs switching frequency. Further, each switching device always conducts for 180˚ (or half cycle) regardless of the pulse width of the quasi-square wave so that this switching method results in equalizing the current stress in each active device. A multilevel inverter has four main advantages over the conventional bipolar inverter. First, the voltage stress on each switch is decreased due to series connection of the switches. Therefore, the rated voltage and consequently the total power of the inverter

could be safely increased. Second, the rate of change of voltage (dv/dt) is decreased due to the lower voltage swing of each switching cycle. Third, harmonic distortion is reduced due to more output levels. Fourth, lower acoustic noise and electromagnetic interference (EMI) is obtained. It consists of a full-bridge inverter circuit and inverter produces output voltage in eleven levels: The advantages of the inverter topology are Improved output voltage quality, Smaller filter size, Lower Electromagnetic interferences, Lower total harmonics distortion compared with conventional eleven level pulse width modulation ,Reduced number of switches compared to the conventional 11-level inverter.

4. Features of Cascaded Multi Level Inverter

For real power conversions, (ac to dc and dc to ac), the cascaded-inverter needs separate dc sources. Connecting separated dc sources between two inverters in a back -to-back fashion is not possible because a short circuit will be introduced when two back -to-back inverters are not switching synchronously.

- Multi level inverter employees the principle of phase control to vary the output voltage.
- They can generate the output voltage with low distortion.
- They reduce the device voltage stress and draw input current with low distortion.
- They can operate at low switching frequency.
- Increasing the output voltage and power does not increase the rating of the device.
- They have no electromagnetic interference.

An n level cascaded H-bridge inverter requires Switching devices=2(n-1) and Voltage source=(n-1)/2.The output voltage is the sum of the voltage that is generated by each cell. The number of output voltage levels are 2*n*+1, where *n* is the number of cells.

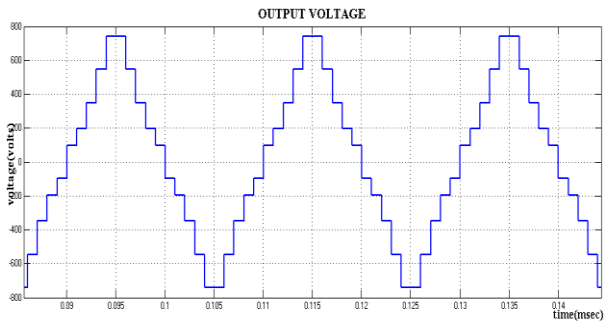

Fig .2 Eleven Level Output Voltage

These topologies are intensively used for high-power applications and standard drives for medium-voltage industrial applications [4]. Solutions with a higher number of output voltage levels have the ability to synthesize waveforms with a better harmonic spectrum and to limit the motor-winding insulation stress. However, increasing the number of devices tends to reduce the overall reliability and efficiency of the power converter.

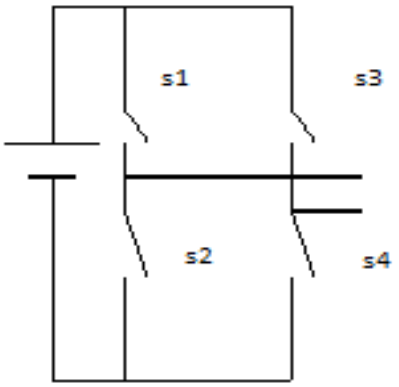

Fig .3 Single Phase of Cascaded Multi level Inverter

Table: 1 Single Phase Cascaded Multi level Inverter

Voltage	S1	S2	S3	S4
V	1	0	0	1
0	0	1	0	1
-V	0	1	1	0

The tabulation of single phase of cascaded multilevel inverter has the output voltages of –v, 0, +v.

5. Simulation and Results

MATLAB Simulink is used to check the performance of the induction motor and also used to improve their performance.

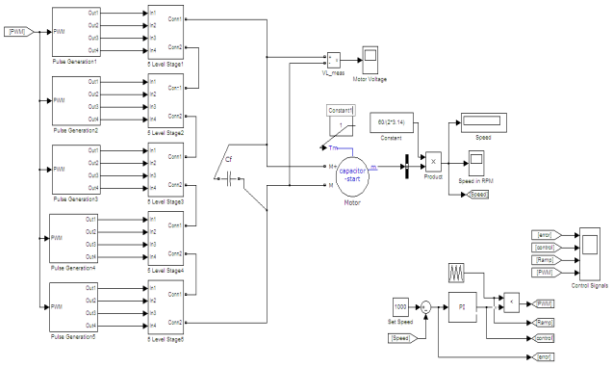

Fig. 4 Closed Loop Simulink Model

Fig. 1 shows the block diagram of 11- Level Inverter Fed Induction Motor. It consists of DC source, 11- level Inverter, Induction motor, Gate pulse generator. This figure shows the overall closed loop simulink model of an eleven level inverter. And the closed loop control is achieved with PI control and the gate pulse is generated using PWM technique.

6.1 Subsystem of Cascaded H-Bridge Topolog

The switches used here are MOSFET. There are five stages for implementing an eleven level inverter and each stage the same topology [5].

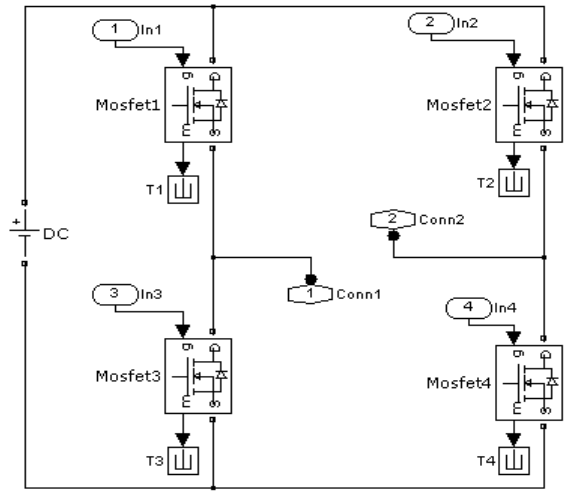

Fig. 5 Subsystem of Cascaded H-Bridge

6.1.1. Subsystem of Pulse generation 1

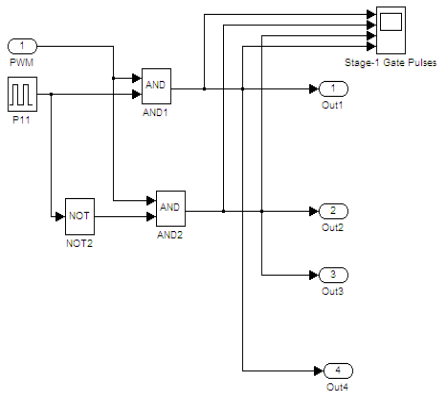

Fig. 6 Subsystem of Pulse Generator

The pulse for the first stage switches is generated using a single pulse generator and PWM signal.

6.1.2. Speed

The speed is settled at the set speed of 1000 rpm using PI control.

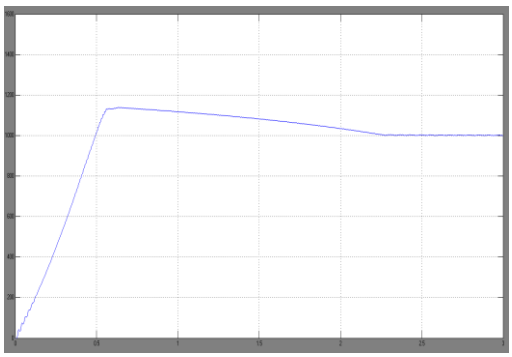

Fig.7 Speed in Closed Loop Control of Eleven Level Inverter

6.1.3 Voltage

An eleven level inverter produces almost a sinusoidal voltage.

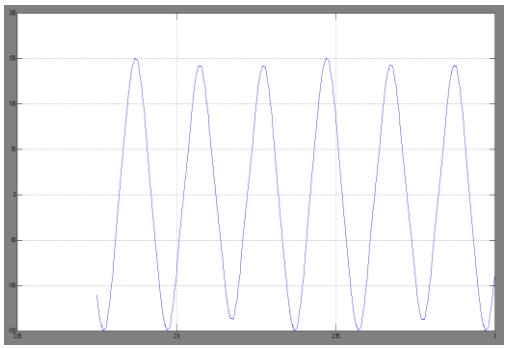

Fig.8 Voltage

6.1.4. Control Signal

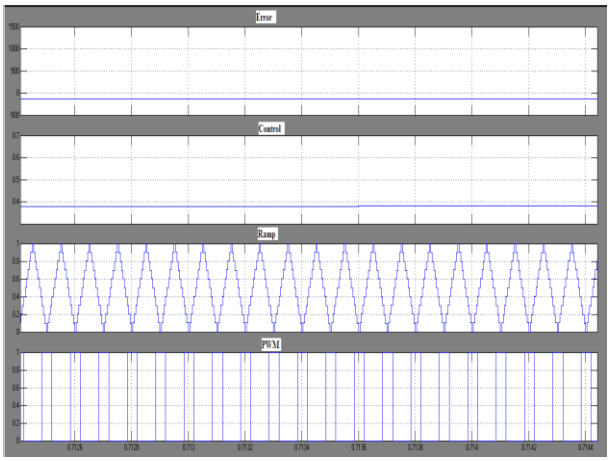

Fig.9 Control Signals

6.1.5 FFT Analysis and THD

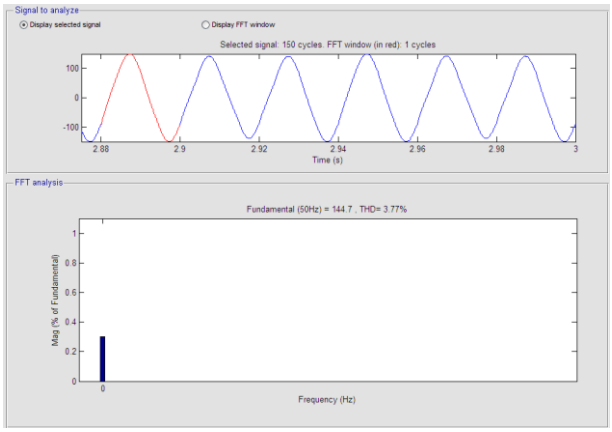

Fig.10 FFT Analysis and THD

The THD has been reduced to 3.77% using the closed loop PI control of an eleven level inverter.

Conclusion & Future Scope

We hereby conclude that Multi-level inverters are a very promising technology in the power industry. In this paper, the advantages and applications of Multi-Level Inverters are mentioned and a detailed description of different multi-level inverter topologies is presented. Single Phase H-Bridge Inverter functioning is realized virtually using MATLAB SIMULINK. A detailed Multi-Level Inverter is presented from which we concluded that the harmonic content is greatly reduced in Multi-Level Inverter. The cascaded H-bridge has the lowest weight and cost between the multilevel inverters, but its power losses is more that all the other topologies.

A single phase Cascade H-Bridge Inverter is designed and implemented practically. The components used in the practical implementation of H-Bridge Inverter are described. The drive system can be used in industries where adjustable speed drives are required to produce output with reduced harmonic content. The simulation results of voltage, current, speed and spectrum are presented.

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